1. A reticle used to make memory cells, said reticle comprising:

at least one generally planar surface defining a plurality of lead line cutouts and a plurality of fill pattern cutouts therein, said plurality of fill pattern cutouts interspersed between said plurality lead line cutouts and spaced apart from each of said plurality of lead line cutouts by an amount sufficient to avoid capacitive communication between a metal lead line and a metal fill pattern formed on a memory cell by said reticle, wherein said plurality of lead line and fill pattern cutouts are disposed in an array within a surface of said reticle such that the periphery of said array is substantially bounded by straight edges and no portion of any of said plurality of fill pattern cutouts within said array extends laterally beyond said periphery; and

a grid defined by at least a portion of said surface, said grid comprising an interconnected series of spaces between each adjacent said plurality of lead line and fill pattern cutouts such that a lateral distance defining the width of any one of said series of spaces is substantially equal to that of any other of said series of spaces within said grid, the longest linear dimension between each of said series of spaces is no longer than the longest dimension of any of said plurality of fill pattern cutouts and no intersection defined by a crossing between any two of said interconnected series of spaces includes uninterrupted linear dimensions.

2. A reticle according to claim 1, wherein at least a portion of said fill pattern cutouts are T-shaped.

3. A reticle according to claim 1, wherein at least one of said plurality of fill pattern cutouts further define a first in-plane dimension and a second in-plane dimension substantially orthogonal to said first in-plane dimension such that at least one of said plurality of fill pattern cutouts overlaps with at least one adjacent fill pattern cutout along at least one of said first or second in-plane dimensions.

4. A reticle according to claim 1, wherein a lateral dimension defining a width of any one of said interconnected series of spaces is substantially the same between all other said series of spaces.

5. A semiconductor fabrication system comprising:

a photoresist application mechanism to deposit photoresist onto a semiconductor substrate;

an electromagnetic radiation source to illuminate at least a portion of said photoresist;

a solvent dispensing mechanism to wash away unexposed photoresist;

an etching mechanism to selectively remove at least one layer of insulative coating; and

a reticle with a generally planar body that occupies first and second substantially orthogonal dimensions; said reticle comprising:

a first segment of said generally planar body defined by a plurality of cutouts therethrough, said cutouts adapted to define topographic peaks on a semiconductor, where said cutouts are shaped to further define at least one lead line and a plurality of dummy patterns spaced apart from one another;

a second segment of said generally planar body comprising the remainder thereof such that a pattern formed by said remainder extends in said first and second substantially orthogonal dimensions, said remainder adapted to define a plurality of interpeak valleys on said semiconductor;

a geometrically simple array defined by said plurality of cutouts, wherein:

the periphery of said array is substantially bounded by straight edges of said first segment; and

no portion of any of said plurality of said dummy patterns within said first segment extends laterally beyond said periphery of said array; and

a grid defined by at least a part of said second segment such that the longest linear dimension in the portion of said second segment bounded by said periphery is no longer than the longest linear dimension of any part of said first segment and no intersection formed in said second segment includes uninterrupted linear dimensions.

6. A method for fabricating a reticle, said method comprising:

producing a plurality of lead line cutouts in a reticle body;

producing a plurality of fill pattern cutouts interspersed between said plurality lead line cutouts, and spaced apart from each of said plurality of lead line cutouts by an amount sufficient

to avoid capacitive communication between a metal lead line and a metal fill pattern formed on a memory cell by said reticle, wherein said plurality of lead line and fill pattern cutouts are disposed in an array within a surface of said reticle such that the periphery of said array is substantially bounded by straight edges and no portion of any of said plurality of fill pattern cutouts within said array extends laterally beyond said periphery; and

forming a grid comprising an interconnected series of spaces between each adjacent said plurality of lead line and fill pattern cutouts, where a lateral distance defining a width of any one of said series of spaces is substantially equal to that of any other of said series of spaces within said grid, such that the longest linear dimension between each of said series of spaces is no longer than the longest dimension of any of said plurality of fill pattern cutouts and no intersection defined by a crossing between any two of said interconnected series of spaces includes uninterrupted linear dimensions.

7. A method according to claim 6, wherein at least a portion of said fill pattern cutouts are T-shaped.

8. A method according to claim 6, wherein at least one of said plurality of fill pattern cutouts overlaps with at least one adjacent fill pattern cutout.